Demonstration of on-chip *Appended* Power Amplifier for Improved Efficiency at Low Power Region

Hyun-Min Park, Sang-Hoon Cheon[1], Jae-Woo Park[1], and Songcheol Hong
Dept. EECS, Korea Advanced Institute of Science and Technology (KAIST)
373-1, Guseong-dong, Yuseong-gu, Daejeon, 305-701, Republic of Korea
[1]Knowledge*on Inc., 513-37, Eoyang-dong, Iksan, 570-210, Republic of Korea

Abstract — **A new power amplifier topology which can achieve improved efficiency at power backoff region is demonstrated in this paper. In this topology, the output stage of the amplifier is appended with a secondary transistor in a parallel way through a 3-port interstage matching circuit and an impedance transforming network. By careful selection of the ratio of device active area, this appended transistor achieves earlier saturation at lower output power level than the output transistor, which is a basic requirement in achieving high efficiency. The power amplifier has been realized with InGaP/GaAs HBT technology and showed efficiency improvement of 81% at output power of 16.7 dBm. The proposed topology enables one-chip integration, hence is very attractive for portable communication terminals.**

I. Introduction

Power amplifier is the one of key elements in communication systems, such as PCS and CDMA, since it directly determines the spectral purity of the output signal. At the same time, due to its high power consumption rate, it is most effective to use a statistically efficient power amplifier on a time scale to increase the overall functionality time [1]-[2]. Especially in mobile communication system such as wireless phone terminal, the efficiency of power amplifier directly affects the talk time, therefore it is highly recommended to use a dynamically efficient one.

A power amplifier with dc-dc converter was introduced in [3]-[5], where the output supply voltage is varied in accordance with the input power level. This makes the transistor operate in near saturation at all power levels, hence generates higher efficiency. However, the additional circuitry restricts the applicability in handheld terminals where the increased complexity results in the increased manufacturing cost. A power amplifier with switched gain stage [6] bypasses the output transistor in power backoff operation with an aid of additional switches which are inserted in the input and output sides of output transistor. As a result, the driver transistor alone generates output power with increased efficiency in low power mode. This is a direct benefit from the innate tradeoff between efficiency and output power when the driver transistor with a smaller active area than the power transistor is used. However, the linearity can be degraded if the switches are integrated with the amplifier circuit monolithically.

In this paper, a new power amplifier configuration which exhibits improved efficiency at power backoff operation is described. The design aims at a single-chip MMIC solution without significantly increasing the number of components. The operating principle as well as measurement data will be shown to demonstrate the benefit of the proposed circuit.

II. Operating Principle

The conceptual topology of the proposed power amplifier is described in Fig. 1. It is very similar to the conventional multistage power amplifier with typical impedance matching circuits except for the appended stage and the impedance transforming network illustrated with the thick lines. The power stage is appended with an auxiliary stage which is connected in parallel with the power stage. This appended stage is constructed with another transistor other than power transistor, but shares the same output matching circuitry with the power stage. Only the appended stage is turned on with the power stage being turned off during low power mode operation.

To drive the appended stage at low power mode, the output signal from the driver stage should be directed to the appended stage. At the same time, the signal into the power stage should be blocked so that it does not turn on the device accidentally. This can be done easily by using monolithic switches since they can be made to exhibit a low loss under ON state and a high isolation under OFF state. However, if one tries to avoid the use of switches, the output signal from the driver stage should be divided into two different paths through the interstage matching circuit. In this case, the sufficient amount of signal isolation cannot be achieved easily with the conventional matching elements. Nevertheless, due to the fact that the turn-on voltage of a GaAs HBT is usually high (> 1.1 V), it is feasible to assume that the power device remains at OFF state up to the signal level that saturates the appended device. Since the power stage is not completely isolated

0-7803-7695-1/03/$17.00 © 2003 IEEE

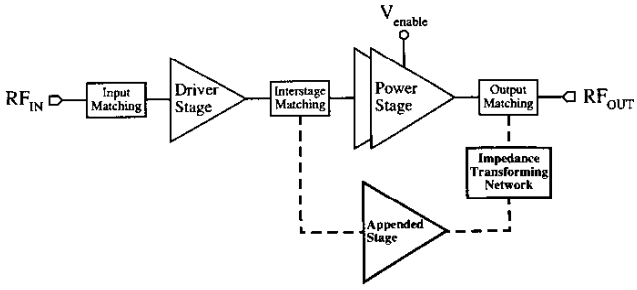

Fig. 1. Conceptual topology of the proposed power amplifier.

from the appended stage in this case, the input impedance of power device should be properly accounted for when designing interstage matching circuit. This can be troublesome compared with the circuit using switches.

On the other hand, to exploit the single output matching circuit, the output signal from the appended stage should be merged into the output side of the power stage in such a way that the output matching also provides the optimum load condition for the appended device. In this case, a direct connection between two devices can hardly produce the optimum load condition. However, it is best to place the merging point as close to the power device as possible to simplify the output matching circuit. The output impedance of the 'OFF' state power device should be also considered here to successfully design the output matching circuit.

In this respect, a 3-port interstage network design is demanded as illustrated in Fig. 2. Γ_{S1} and Γ_{S2} represent the source impedances of power transistor and appended transistor while Γ_{L3_low} and Γ_{L3_high} represent the desired load conditions for the driver transistor at low and high power modes, respectively. Γ_{L3_low} and Γ_{L3_high} can not be designed to have the same value for both modes since the power device is turned off at low power mode. This means that Γ_{S1} at low power mode (Γ_{S1_low}) is different from Γ_{S1} at high power mode (Γ_{S1_high}). Fortunately, it is possible to design Γ_{L3_low} for maximum efficiency operation and Γ_{L3_high} for maximum gain operation for the driver device since these load conditions are usually different from each other. It is noted that matching Γ_{L3_low} for maximum efficiency is beneficial in maximizing the overall efficiency at low power mode.

After determining the most suitable topology for the interstage matching, the components are optimized with the remaining ports being terminated with the input impedance of the devices according to their bias conditions. Due to the complexity of the interstage matching, it is usually required to employ more elements than a conventional 1-section LPF or HPF topology. Therefore, the signal loss can be slightly higher in this type of interstage matching.

As a consequence of the described design methodology,

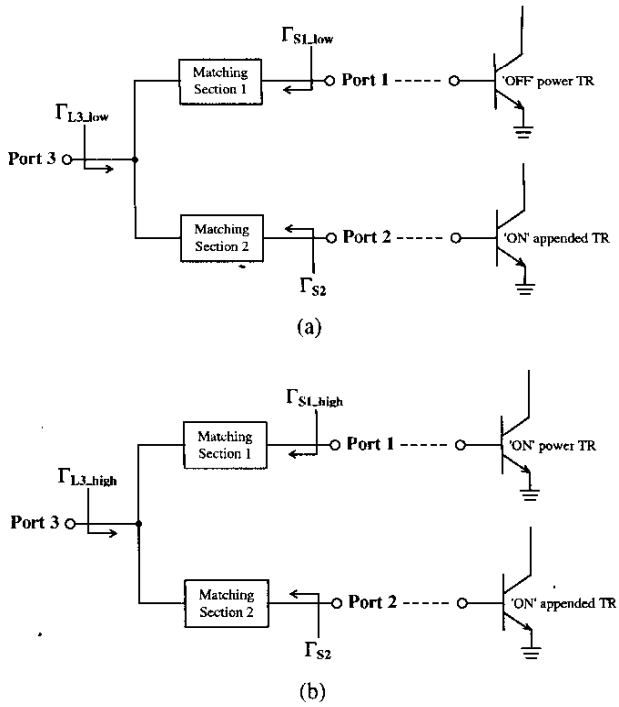

Fig. 2. Illustration of 3-port interstage network design in (a) low and (b) high power modes.

the majority of output signal from the driver stage is applied to the power stage. Only a small portion of the signal, which is sampled through an interstage matching network, is applied to the appended stage. This sampling ratio is a major contributor in determining the gain difference between low power and high power modes.

The transistor used in the appended stage usually has the smaller active area than the power transistor hence becomes saturated at lower power level. This is an underlying principle for improved efficiency at low power mode since a saturated device exhibits a higher efficiency. The area of the appended transistor can be chosen plausibly based on which power level the efficiency needs to be improved.

The impedance transforming network is inserted between the two transistors to optimize the load condition for the appended transistor. Therefore, this network is usually configured to be in series with the output matching network, and provides higher load impedance to the appended transistor. As a result, the entire circuit experiences a premature saturation at sufficiently backed off region at low power mode.

When the power stage is turned on at high power mode, most of the signal will be transferred to the output terminal via output matching circuit. The signal leakage back into the appended stage can be neglected since the impedance

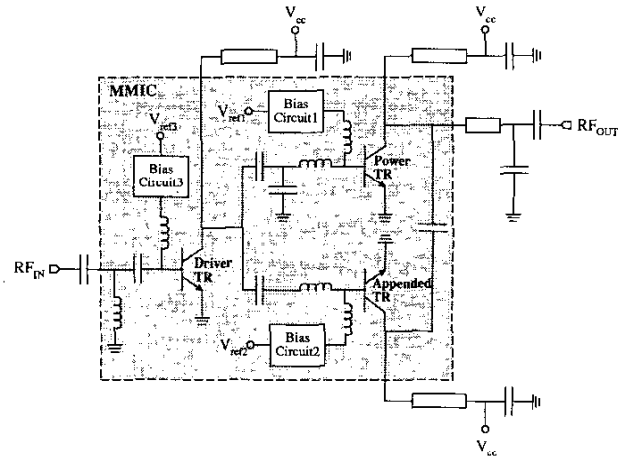

Fig. 3. Schematic diagram of the fabricated InGaP/GaAs power amplifier.

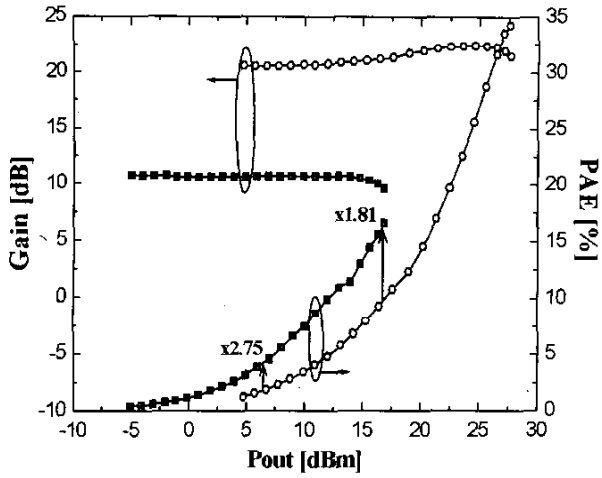

Fig. 4. The measured efficiency and gain of InGaP/GaAs HBT power amplifier at 1.75 GHz (filled symbol – low power mode, open symbol – high power mode).

presented by the transforming network is much higher than the one by the output matching circuit.

Since the proposed topology does not require additional components other than transistors, it is very practical for one-chip integration without much increasing manufacturing cost. Finally, more stages can be appended when one needs to improve efficiency over a broader power range.

III. Measurement

The power amplifier was realized with InGaP/GaAs HBT technology. 12, 48, and 12 finger devices with a unit emitter area of 2x20 μm^2 were used for the driver, power, and appended stages, respectively. The detailed schematic of the circuit is displayed in Fig. 3. The impedance transforming network is constructed with a series capacitance. This is very effective in terms of reducing the chip size as well as achieving dc blocking. Current mirror circuit was used for biasing transistors in each stage. The bias current level can be tuned to a desired value by controlling the reference voltage (Vref) in the bias circuit. Also, each stage can be turned off completely by setting Vref to 0 V. Input matching, interstage matching, and impedance transforming networks were integrated in a single chip while the output matching was done off-chip to minimize the signal loss.

Fig. 4 shows the measured results of the fabricated power amplifier at 1.75 GHz. The bias current was set to 10 and 40 mA for 12 and 48 finger HBTs, respectively, and Vcc was set to 3.3 V. In low power mode operation, P_{1dB} of 16.7 dBm was obtained with an associated PAE of 16.4 % while in high power mode, P_{1dB} was 27.6 dBm with PAE of 34.2 %. It is noted that PAE is improved by a factor of at least 1.81 over a broad range of output power. The maximum improvement of x2.75 was obtained at output power of 6.3 dBm. The measured small-signal gains of both modes were 10.8 dB and 20.5 dB, respectively. Consequently, it is proven that power amplifier can be designed to operate at higher efficiency over a broad range of output power levels by using the proposed topology.

IV. Conclusion

A novel architecture of power amplifier for improved efficiency at low power region is introduced. This has been verified with the fabricated InGaP/GaAs HBT MMIC power amplifier. Efficiency improvement over a broad power range was achieved with a maximum improvement occurring at a Pout of 6.3 dBm. The design issues related to the interstage and the output matching circuits were discussed. This architecture is very attractive in mobile communication system such as handheld phone terminals.

Acknowledgement

The authors wish to acknowledge the support from Knowledge*on Inc., Iksan, Korea, for the fabrication of HBT MMIC power amplifier. This work was partly supported by KOSEF under the ERC program through the MINT research center at Dongguk University.

References

[1] Thomas Fowler, Kerry Burger, Nai-Shuo Cheng, Apostolos Samelis, Ede Enobakhare, and Stephan Rohlfing, "Efficiency improvement techniques at low power levels for linear

CDMA and WCDMA power amplifiers," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, 2002, pp. 41-44.

[2] J. Staudinger, "An overview of efficiency enhancements with application to linear handset power amplifiers," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, 2002, pp. 45-48.

[3] Gary Hanington, Pin-Fan Chen, Peter M. Asbeck, and Lawrence E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 1471-1476, Aug. 1999.

[4] T. B. Nishimura, N. Iwata, and G. Hau, "Wide-band CDMA highly-efficient heterojunction FET over wide range output power with DC-DC converter," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1999, pp. 1091-1094.

[5] Kyounghoon Yang, George I. Haddad, and Jack R. East, "High-efficiency class-A power amplifiers with a dual-bias-control scheme," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 1426-1432, Aug. 1999.

[6] Joe Staudinger, "Stage bypassing in multi-stage PAs," *IEEE MTT-S Symposium Workshop on Efficiency & Linearity Enhancement Methods for Portable RF/MW Power Amplifier*, Jun. 2000.